

S206N-A Miniaturized High Precision Chip of Beidou-3

specification
V1. 2-20240806

Catalogue

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1. Product Introduction



Figure 1 Product Appearance Diagram

The S206N-A miniaturized Beidou-3 high-precision chip is a domestically developed, globally compatible, multi-mode, multi-frequency baseband RF integrated automotive-grade high-precision chip (hereinafter referred to as "S206N-A"). Featuring a highly integrated design, it combines anti-interference capabilities, low power consumption, and miniaturization. With minimal peripheral components and a compact carrier area, it delivers complete receiver functionality, reducing system design complexity, shortening development cycles, and lowering hardware costs for users.

The S206N-A is widely applicable in autonomous driving, lane-level navigation, road rescue, and V2X systems.

2. Product Features

- Supports BDS, GPS, GLONASS, GALILEO signals across all system and frequency bands, as well as SBAS signals, and features BeiDou ground-based augmentation network functionality.
- Supports fast, high-precision positioning across all frequency bands, including onboard high-frequency RTK and PPP positioning.
- It has the ability of deep coupling combination navigation;
- Complies with the requirements of AEC-Q100 Grade 2 standards.
- The system integrates high-capacity, low-power dynamic random access memory (DRAM, 32 MB) and non-volatile memory (NVM, 8 MB) within the same device.
- Featuring a built-in high-performance processor with 800MHz clock speed and advanced floating-point capabilities.
- The maximum data update rate is 100Hz.
- 10mm×8mm small package.

3. Encapsulation Size

The plastic BGA 192 pin package is used. The pin center distance is 0.6mm, the ball diameter is 0.3mm, and the package size is 10mm (length) × 8mm (width) × 1.52mm (height). The external size is shown in Figure 2, and the dimensional tolerance is shown in Table 1.

Table 1 Device Package Dimension Tolerance Table

Dimension Symbol	Dimension value (unit: mm)		
	Minimum	Nominal	Maximum
A	1.37	1.52	1.67
D	7.9	8.0	8.1
E	9.9	10.0	10.1

Dimension Symbol	Dimension value (unit: mm)		
	Minimum	Nominal	Maximum
D1	6.55	6.60	6.65
E1	8.95	9.00	9.05
e	0.60		
b	0.25	0.30	0.35

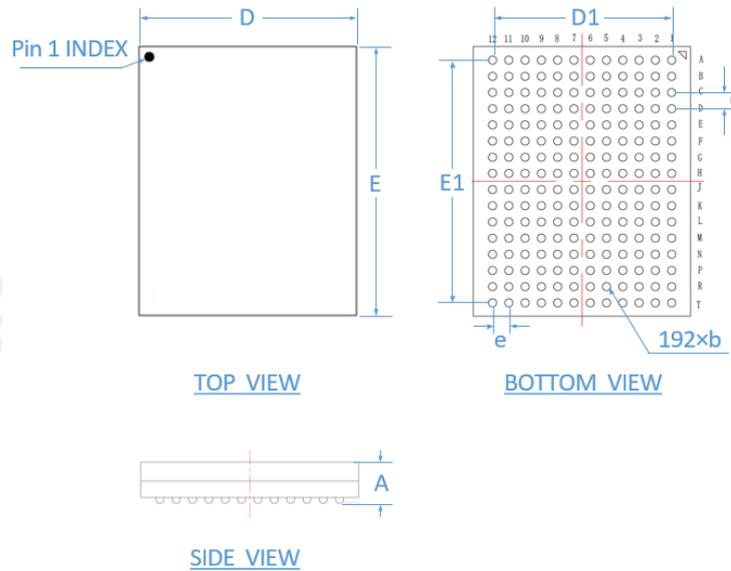


Figure 2 Device外形 Dimensions Diagram

4. Qualification

Table 2 Key Performance Indicators

Performance index		
Number of channels		384
Star frequency	BDS	B1I、B2I、B3I、B1C、B2a、B2b
	GPS	L1C/A、L2C、L5、L1C
	GLONASS	L1、L2
	Galileo	E1、E5a、E5b
	QZSS	L1、L2
	SBAS	L1 C/A
Single point positioning accuracy	Plane	≤ 1.5m (RMS)
	Altitude	≤ 3.0m (RMS)
DGNSS accuracy	Plane	≤ 0.3m + 10ppm (RMS)
	Altitude	≤ 0.6m + 10ppm (RMS)
RTK accuracy	Plane	≤ 1cm + 1ppm (RMS)
	Altitude	≤ 2cm + 1ppm (RMS)

Time synchronization accuracy	≤ 20ns (RMS)	
Rate accuracy	≤ 0.05m/s (RMS)	
Cold start time	≤ 35s	
Hot start time	≤ 5s	
Re-capture time	≤ 1s	
RTK initialization time	≤ 5s (10 km baseline)	
Support protocol	RTCM2.X RTCM3.X NMEA-0183	
Typical power consumption	Low power consumption <500mW, BeiDou RNSS full frequency point <800mW	
Data rate	PVT	1Hz, 2Hz, 5Hz, 10Hz,
	RTK	1Hz, 2Hz, 5Hz, 10Hz,
	PPP-RTK	1Hz, 2Hz, 5Hz, 10Hz,
	RAW	1Hz, 2Hz, 5Hz, 10Hz,
	DR	100Hz
Physical characteristics		
Size	10mm × 8mm × 1.52mm	
Environment pointer		
Working temperature	-40°C ~ +105°C	
Storage temperature	-55°C ~ +125°C	
Chip interface		
Functional interface	UART, I ² C, PPS, SPI, GPIO, ODO, etc.	
Note: The final application performance is subject to the actual firmware loaded.		

5. Pin Definition

The pin names and descriptions are shown in the table below.

Table 3 Device Package Pin Names and Descriptions

Pin number	Pin name	Pin type	Pin function description
A11、B12、C3、C5、C7、C11、D4、D6、D8、D10、D12、E3、E5、E7、E9、E11、F4、F6、F8、F12、J8、J12、K10、M8、P9、T9、T10、T12	VSS	Reference site	Digital signal reference ground
J1、J5、J6、K2、K5、K7、L1、L6、M3、N4、N8、P1、P3、P5、P6、R2、R4、R6、T2、T4、T6、T8	GND_RF	Reference site	RF reference ground
B11、C12、E12、F11、G12	+1.2V_VDDRQ	Power input	DDR 1.2V power supply
D3、D5、D7、E4、E6、E8、F5、F7	VDD_CORE	Power input	Core logic power supply
H12	+1.8V_VDDR	Power input	DDR 1.8V power supply

Pin number	Pin name	Pin type	Pin function description
C4	ADC_AVDD	Power input	ADC analog power supply
C2	ADC_AVDDIO	Power input	ADC IO 1.8V power supply
C6	ADC_DVDD	Power input	ADC digital power supply
C9	AON_GPIO_0	/	Keep pin, default NC
C8	AON_GPIO_1	/	Keep pin, default NC
G4	AVDD08_LDO	Power output	RTCLDO0.8V output
F3	AVDD18_LDO	Power output	RTCLDO1.8V output
G5	AVDD33_LDO	Power input	RTC LDO 3.3V Input
A12	BP_ZQ	O	ZQ calibration, 240 ohm 1% resistance for ground connection
P12	BPSK/GPIO_D26	I/O	RDSSTX output /GPIO
M7	BYPASS_VCO	I/O	Bandgap filter, with a 10 nF filter capacitor
K6	CLKINOUT	O	ADC sampling clock, AC signal, load capacitance <5pF
M10	EXT_LAT0/GPIO_D24	I/O	External latch-in/gpio
K1	FREF	I	RF reference clock input, reference clock amplitude 0.6~1.2Vpp
E1	GPIO0/UART3_RXD	I/O	GPIO/UART3 RX with interrupt capability
D1	GPIO1/UART3_TXD	I/O	GPIO/UART3 TX with interrupt capability
F1	GPIO2/UART6_RXD	I/O	Interrupt-enabled GPIO/UART6 RX
H4	GPIO3/UART6_TXD	I/O	GPIO/UART6 TX with interrupt capability
G2	GPIO4/UART6_CTS	I/O	GPIO/UART6 CTS with interrupt capability
H3	GPIO5/UART6_RTS	I/O	Interrupt-enabled GPIO/UART6 RTS
H2	GPIO6/UART7_RXD	I/O	GPIO/UART7 RX with interrupt capability
J7	GPIO7/UART7_TXD	I/O	GPIO/UART7 TX with interrupt capability
K8	GPIO8	I/O	GPIO with interrupt capability
K9	GPIO9	I/O	GPIO with interrupt capability
M9	I2C0_SCL/GPIO_A24	I/O	I2C clock/GPIO with interrupt capability
L9	I2C0_SDA/GPIO_A25	I/O	I2C data/GPIO with interrupt capability

Pin number	Pin name	Pin type	Pin function description
B4	IF_AIN_I0_N	I	Baseband ADC CH0 I-channel analog input N terminal
A4	IF_AIN_I0_P	I	Baseband ADC CH0 I-channel analog input P terminal
B6	IF_AIN_I1_N	I	Baseband ADC CH1 I-channel analog input N terminal
A6	IF_AIN_I1_P	I	Baseband ADC CH1 I-channel analog input P terminal
B8	IF_AIN_I2_N	I	Baseband ADC CH2 I-channel analog input N terminal
A8	IF_AIN_I2_P	I	Baseband ADC CH2 I-channel analog input P terminal
B10	IF_AIN_I3_N	I	Baseband ADC CH3 I analog input N terminal
A10	IF_AIN_I3_P	I	Baseband ADC CH3 I analog input P terminal
B3	IF_AIN_Q0_N	I	Baseband ADC CH0 Q-channel analog input N terminal
A3	IF_AIN_Q0_P	I	Baseband ADC CH0 Q-channel analog input P terminal
B5	IF_AIN_Q1_N	I	Baseband ADC CH1 Q-channel analog input N terminal
A5	IF_AIN_Q1_P	I	Baseband ADC CH1 Q-channel analog input P terminal
B7	IF_AIN_Q2_N	I	Baseband ADC CH2 Q-channel analog input N terminal
A7	IF_AIN_Q2_P	I	Baseband ADC CH2 Q-channel analog input P terminal
B9	IF_AIN_Q3_N	I	Baseband ADC CH3 Q-channel analog input N terminal
A9	IF_AIN_Q3_P	I	Baseband ADC CH3 Q-channel analog input P terminal
M6	IFOUTN_C1I	O	RF channel 1 analog intermediate frequency output I channel N terminal
M5	IFOUTN_C1Q	O	RF channel 1 analog intermediate frequency output Q-channel N-terminal
L3	IFOUTN_C2I	O	RF channel 2 analog intermediate frequency output I-channel N-terminal
L4	IFOUTN_C2Q	O	RF channel 2 analog intermediate frequency output Q-channel N-terminal

Pin number	Pin name	Pin type	Pin function description
N1	IFOUTN_C3I	O	RF channel 3 analog intermediate frequency output I-channel N-terminal
M1	IFOUTN_C3Q	O	RF channel 3 analog intermediate frequency output Q-channel N-terminal
N6	IFOUTP_C1I	O	RF channel 1 analog intermediate frequency output I-channel P-terminal
N5	IFOUTP_C1Q	O	RF channel 1 analog intermediate frequency output Q-channel P-terminal
K3	IFOUTP_C2I	O	RF channel 2 analog intermediate frequency output I-channel P-terminal
K4	IFOUTP_C2Q	O	RF channel 2 analog intermediate frequency output Q-channel P-terminal
N2	IFOUTP_C3I	O	RF channel 3 analog intermediate frequency output I-channel P-terminal
M2	IFOUTP_C3Q	O	RF channel 3 analog intermediate frequency output Q-channel P-terminal
H11	LPDDR2_ZQ	O	ZQ calibration, 240 ohm 1% resistance for ground connection
L12	ODO_DIR/GPIO_C24	I/O	Gauge direction input/GPIO
J11	ODO_PULSE/GPIO_C23	I/O	Gauge Pulse Input/GPIO
F10	PLL_AON_AVDD	Power input	PLL 1.8V Analog Power Supply
G8	PLL_AVDD	Power input	PLL 1.8V Analog Power Supply
N11	POWER_OK	I	Reset signal, input low level valid
M11	PPS0/GPIO_D22	I/O	Second Pulse Output/GPIO
D2	PVDD_IF	Power input	1.8V IO power supply for digital intermediate frequency
E2	PVDD18_32K	Power input	RTC CLK IO 1.8V power supply
E10	PVDD18_AON	Power input	1.8V IO power supply
B1	PVDD18_CLK	Power input	1.8V clock power supply
G6	PVDD18_Q0	Power input	1.8V IO power supply
K12	PVDD18_Q1	Power input	1.8V IO power supply
F2	PVDD33_32K	Power input	RTC CLK IO 3.3V power supply
C10	PVDD33_AON	Power input	3.3V IO power supply
B2	PVDD33_CLK	Power input	3.3V clock power supply
G7	PVDD33_Q0	Power input	3.3V IO power supply
G11	PVDD33_Q1	Power input	3.3V IO power supply
P7	PWR_ADC_D2S	I	Simulation of the hard-wired configuration pin of the intermediate frequency output mode control
A2	RD_CLK	I	RDSS sampling clock
J4	RF_SCLK	I	Radio frequency SPI clock input, recommended frequency range: 50 KHz to 10MHz

Pin number	Pin name	Pin type	Pin function description
J3	RF_SDATA	I/O	Radio Frequency SPI Data Input/Output Port
J2	RF_SEN	I	Enable RF SPI, digital logic circuit, and match with IO voltage (VBAT_IO)
T5	RFN_C1	I	Channel 1 RF input N terminal
T3	RFN_C2	I	Channel 2 RF input N terminal
T1	RFN_C3	I	Channel 3 RF input N terminal
R5	RFP_C1	I	Channel 1 RF input P port
R3	RFP_C2	I	Channel 2 RF input P port
R1	RFP_C3	I	Channel 3 RF input P port
A1	RN_CLK	I	RNSS sampling clock
R11	SIM_CLK/GPIO_A28	I/O	SIM card clock/GPIO with interrupt capability
R12	SIM_IO/GPIO_A29	I/O	SIM card data/GPIO with interrupt function
R10	SIM_RST	O	SIM card reset
H8	SPI0_CLK/GPIO_A30	I/O	SPI Master Controller 0 Clock/Interrupt-enabled GPIO
H5	SPI0_CSN0/GPIO_A31	I/O	SPI main controller 0 chip select 0/GPIO with interrupt capability
H7	SPI0_MISO/GPIO_B0	I/O	SPI Master Controller 0 Data Input/GPIO
H6	SPI0_MOSI/GPIO_B1	I/O	SPI Master Controller 0 Data Output/GPIO
J10	SPI1_CLK/GPIO_B2	I/O	SPI Master Controller 1 Clock/GPIO
J9	SPI1_CSN0/GPIO_B3	I/O	SPI Master Controller 1 Pin Select 0/GPIO
H9	SPI1_MISO/GPIO_B5	I/O	SPI Main Controller 1 Data Input/GPIO
G9	SPI1_MOSI/GPIO_B6	I/O	SPI Main Controller 1 Data Output/GPIO
R9	STRAP_0	I	Enable software setting 0
N9	STRAP_1	I	Enable software setting 1
P10	STRAP_2	I	Enable software setting 2
P11	STRAP_3	I	Enable software setting 3
T11	STRAP_4	I	Enable software setting bit 4
L10	SWPWM0/GPIO_C21	I/O	PWM signal output/GPIO
F9	SYS_CLK	I	The Soc system reference clock input defaults to 20MHz (configurable)

Pin number	Pin name	Pin type	Pin function description
N10	SYS_RSTN	I	Configure the pin to pull up to 3.3V on a 10K resistor by default
H10	UART0_RXD/GPIO_B27	I/O	UART0 RX, Boot loader serial port/GPIO
G10	UART0_TXD/GPIO_B26	I/O	UART0 TX, Boot loader serial port/GPIO
L11	UART1_RXD/GPIO_B29	I/O	Serial port UART1 RX/GPIO
K11	UART1_TXD/GPIO_B28	I/O	Serial port UART1 TX/GPIO
N12	UART2_RXD/GPIO_B31	I/O	Serial port UART2RX/GPIO
M12	UART2_TXD/GPIO_B30	I/O	Serial port UART2 TX/GPIO
N3	VBAT	Power input	RF VCO and IF power supply, 1.8~3.3V
P2	VBAT_DIG	Power input	Radio frequency circuit digital domain power supply, 1.8~3.3V
M4	VBAT_IO	Power input	The RF circuit IO domain power supply defaults to 1.8V
L2	VCC_DIG	Power output	RF circuit with LDO output and external 2.2μF capacitor
L7	VCC_DIG_ADC	Power output	RF circuit with LDO output and external 2.2μF capacitor
L8	VCC_FLASH	Power input	Non-volatile memory power supply 3.3V
L5	VCC_OBUFF	Power output	The OBUFF LDO output is connected to a 2.2uF filter capacitor.
P8	VCC_VCO_C1	Power output	VCO_C1 LDO output, connected to a 2.2uF filter capacitor
R8	VCC_VCO_C2	Power output	VCO_C2 LDO output, connected to a 2.2uF filter capacitor
N7	VCC_VCO_C3	Power output	VCO_C3 LDO output, connected to a 2.2uF filter capacitor
D9	VDD_AON	Power input	Core logic power supply
G3	VDD_RTC	Power input	RTC logic power supply
D11	VDDR_VREF	DDR reference voltage	DDR reference voltage, $+1.2V \cdot \frac{VDDRQ}{2}$
R7	VTUNE_C1	I	External loop filter
T7	VTUNE_C2	I	External loop filter
P4	VTUNE_C3	I	External loop filter
G1	XI	I	RTC crystal oscillator input
C1	XIN	I	External RTC clock input, grounded with a 1M resistor when not in use
H1	XO	O	RTC crystal oscillator output

The mapping diagram of the above pins is shown in the figure below.

	1	2	3	4	5	6	7	8	9	10	11	12
A	RN_CLK	RD_CLK	IF_AIN_Q 0 P	IF_AIN_I 0 P	IF_AIN_Q 1 P	IF_AIN_I 1 P	IF_AIN_Q 2 P	IF_AIN_I 2 P	IF_AIN_Q 3 P	IF_AIN_I 3 P	VSS	BP_ZQ
B	PVDD18_C LK	PVDD33_C LK	IF_AIN_Q 0 N	IF_AIN_I 0 N	IF_AIN_Q 1 N	IF_AIN_I 1 N	IF_AIN_Q 2 N	IF_AIN_I 2 N	IF_AIN_Q 3 N	IF_AIN_I 3 N	+1.2V_VD DRQ	VSS
C	XIN	ADC_AVDD IO	VSS	ADC_AVDD	VSS	ADC_DVDD	VSS	AON_GPIO 1	AON_GPIO 0	PVDD33_A ON	VSS	+1.2V_VD DRQ
D	GPI01	PVDD_IF	VDD_CORE	VSS	VDD_CORE	VSS	VDD_CORE	VSS	VDD_AON	VSS	VDDR_VRE F	VSS
E	GPI00	PVDD18_3 2K	VSS	VDD_CORE	VSS	VDD_CORE	VSS	VDD_CORE	VSS	PVDD18_A ON	VSS	+1.2V_VD DRQ
F	GPI02	PVDD33_3 2K	AVDD18_L DO	VSS	VDD_CORE	VSS	VDD_CORE	VSS	SYS_CLK	PLL_AON_ AVDD	+1.2V_VD DRQ	VSS
G	XI	GPI04	VDD_RTC	AVDD08_L DO	AVDD33_L DO	PVDD18_Q 0	PVDD33_Q 0	PLL_AVDD	SPI1_MOS I	UART0_TX D	PVDD33_Q 1	+1.2V_VD DRQ
H	XO	GPI06	GPI05	GPI03	SPIO_CSN 0	SPIO_MOS I	SPIO_MIS 0	SPT0_CLK	SPI1_MIS 0	UART0_RX D	LPDDR2_Z Q	+1.8V_VD DR
J	RF_GND	RF_SEN	RF_SDATA	RF_SCLK	RF_GND	RF_GND	GPI07	VSS	SPI1_CSN 0	SPI1_CLK	ODO_PULS E	VSS
K	FREF	RF_GND	IFOUTP_C 2I	IFOUTP_C 2Q	RF_GND	CLKINOUT	RF_GND	GPI08	GPI09	VSS	UART1_TX D	PVDD18_Q 1
L	RF_GND	VCC_DIG	IFOUTN_C 2I	IFOUTN_C 2Q	VCC_OBUF F	RF_GND	VCC_DIG_ ADC	VCC_FLAS H	I2CO_SDA	SWPMMO	UART1_RX D	ODO_DIR
M	IFOUTN_C 3Q	IFOUTP_C 3Q	RF_GND	VBAT_IO	IFOUTN_C 1Q	IFOUTN_C 1I	BYPASS_V CO	VSS	I2CO_SCL	EXT_LAT0	PPS0	UART2_TX D
N	IFOUTN_C 3I	IFOUTP_C 3I	VBAT	RF_GND	IFOUTP_C 1Q	IFOUTP_C 1I	VCC_VCO_ C3	RF_GND	STRAP_1	SYS_RSTN	POWER_OK	UART2_RX D
P	RF_GND	VBAT_DIG	RF_GND	VTUNE_C3	RF_GND	RF_GND	PWR_ADC_ D2S	VCC_VCO_ C1	VSS	STRAP_2	STRAP_3	BPSK
R	RFP_C3	RF_GND	RFP_C2	RF_GND	RFP_C1	RF_GND	VTUNE_C1	VCC_VCO_ C2	STRAP_0	SIM_RST	SIM_CLK	SIM_IO
T	RFN_C3	RF_GND	RFN_C2	RF_GND	RFN_C1	RF_GND	VTUNE_C2	RF_GND	VSS	VSS	STRAP_4	VSS

Figure 3 Pin Mapping Diagram

6. Product Label

See the product image below.



Figure 4 Product Identification

7. Order Information

Table 4 Order Information Table

Model	Pack
S206N-A	Antistatic vacuum tray packaging, 264 pieces per tray

Revision History Record of Revision

Order number	Documentation Edition	Revision	Date of issue
1	V1.0	Found	2023.12
2	V1.1	Add pins and product labels	2024.4
3	V1.2	Update product features and performance table	2024.8

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